

Notice of Allowability

Application No.

10/720,315

Examiner

Mehdi Namazi

Applicant(s)

MATSUURA ET AL.

Art Unit

2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to applicant's request for reconsideration and interview on 3 October 2007.
2. ☒ The allowed claim(s) is/are 1,2,4-7 and 9.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

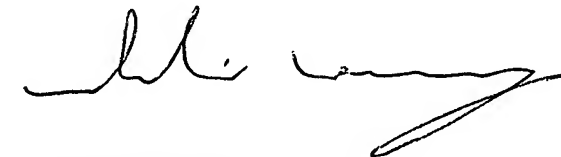
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material

5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 10/3/2007.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



DETAILED ACTION

This office action is in response to applicant's request for reconsideration filed 14 September 2007.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dexter Chang (Reg. No. 44,071) on 3 October 2007.

The application has been amended as follows:

In the Title:

Replace "multiprocessor system" with --multiprocessor system having a shared memory--.

In the Claims:

1. (currently amended) A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:

said common memory is provided with a number of data areas that store data mad with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit for storing same data and same control information as those stored in the common memory and with an access controller; [and]

the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts, from the common bus, data written to said common memory and data lead from said common memory and stores this data in a memory area, which is designated by [said] an address, of the storage unit within its own processor[.]; and

wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

3. canceled.

6. (currently amended) A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:

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said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit for storing same control information as that stored in said control information area and with an access controller; and

the access controller of a processor that does not have access privilege monitors control information and addresses that flow on the common bus, accepts this control information from the common bus and stores it in a memory area, which is designated by [said] an address, of the storage unit within its own processor[.] ; and

wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

8. Canceled.

9. (currently amended) A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:

said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit for storing same data as that stored in said data area and with an access controller; [and]

the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts this data from the common bus and stores it in a memory area, which is designated by [said] an address, of the storage unit within its own processor[.] ; and

wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

Reason for Allowance

The following is an examiner's statement of reasons for allowance: the prior art of the record fails to teach the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts data from the common bus and stores it in a memory area, which is designated by an address, of the storage unit within its own processor; and

wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

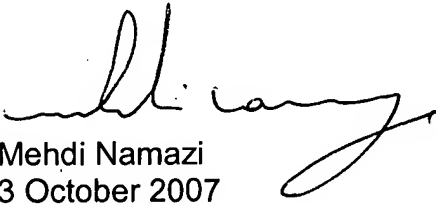
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

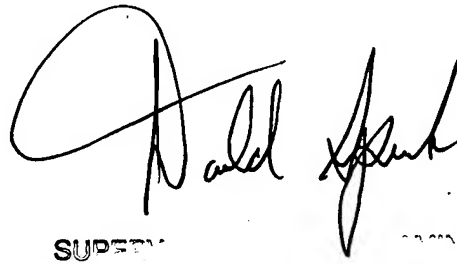
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Mehdi Namazi
3 October 2007



David J. Smith
SUPERVISOR